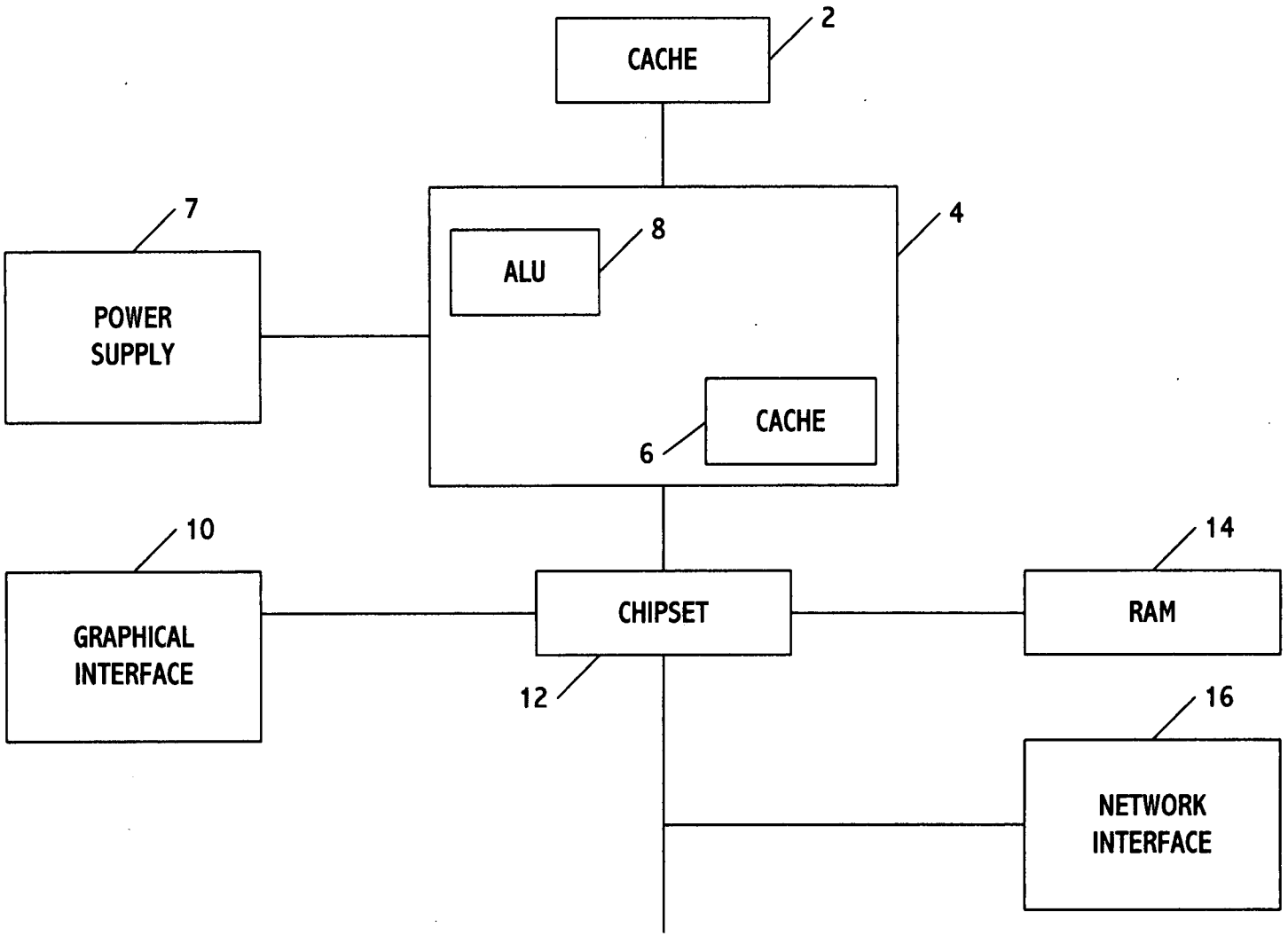
CACHE
2
7
POWER SUPPLY
ALU
8
4
CACHE
6
10
GRAPHICAL INTERFACE
CHIPSET
12
14
RAM
16
NETWORK INTERFACE

FIG. 1

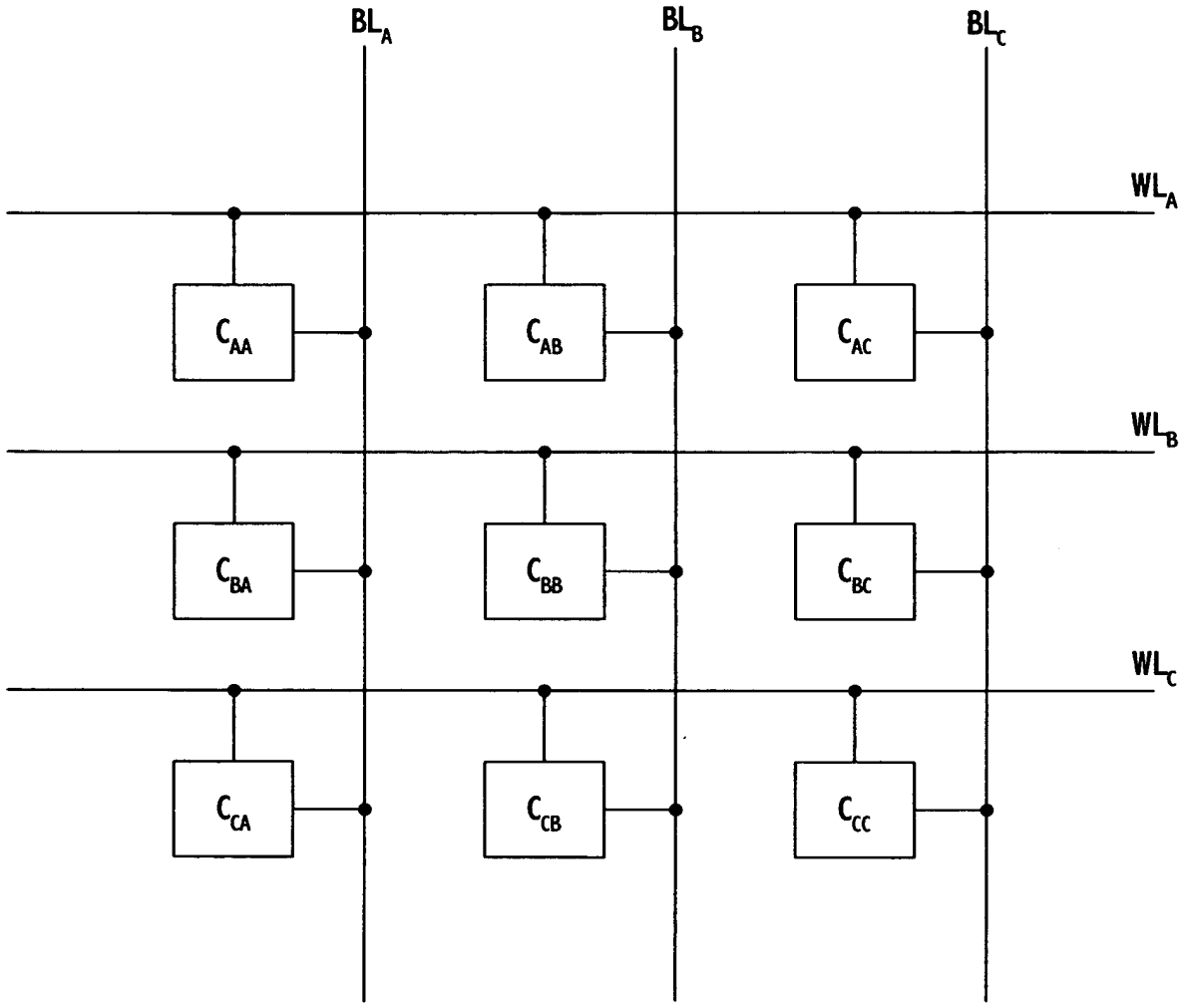

FIG. 2

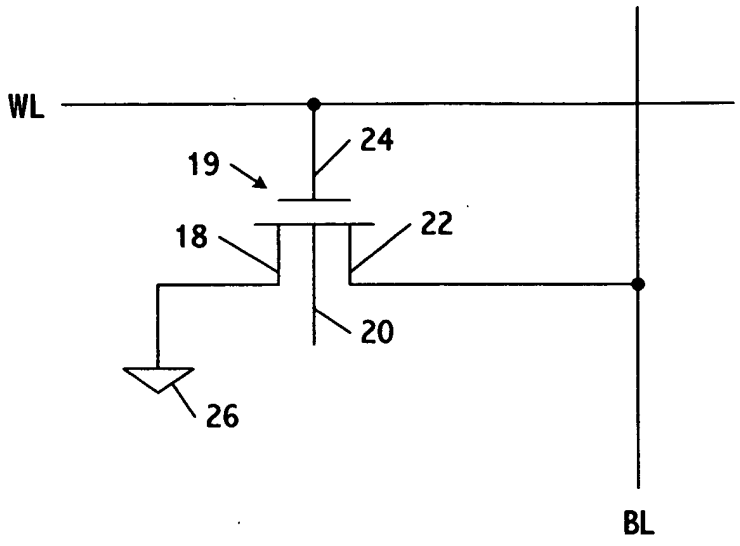

FIG. 3A

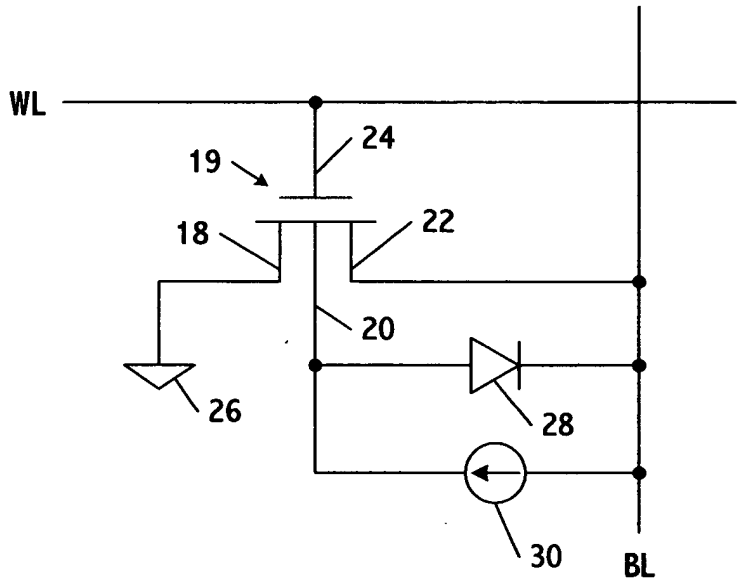

FIG. 3B

	SECOND CHANNEL INTERFACE	GATE (WL)	FIRST CHANNEL INTERFACE (BL)
HOLD	LOW	VERY LOW	VERY LOW, LOW, OR HIGH
WRITE LOGICAL 0	LOW	HIGH	VERY LOW
WRITE LOGICAL 1	LOW	HIGH	HIGH

FIG. 4

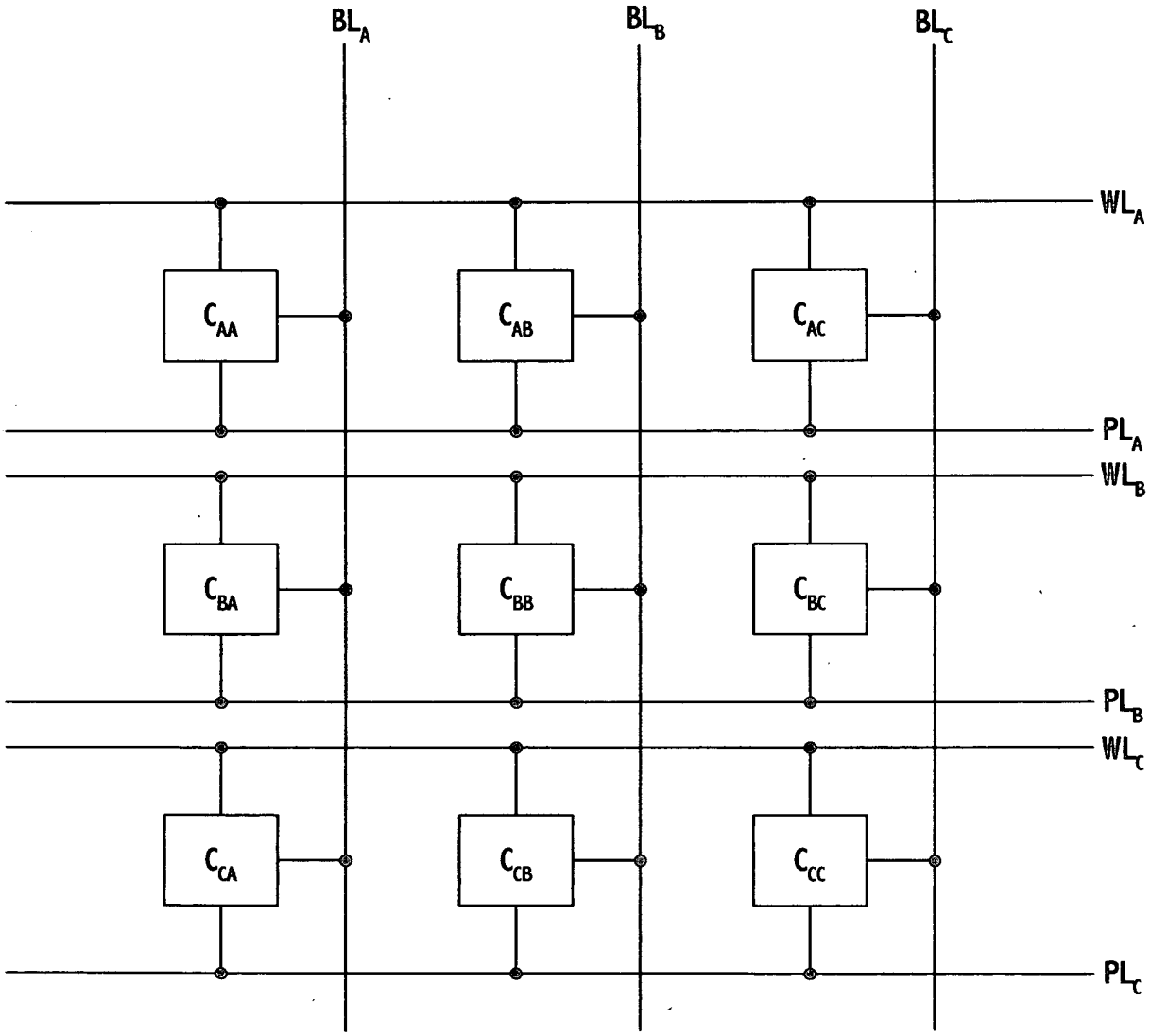
BL_A
BL_B
BL_C
WL_A
C_AA
C_AB
C_AC
PL_A
WL_B
C_BA
C_BB
C_BC
PL_B
WL_C
C_CA
C_CB
C_CC
PL_C

FIG. 5

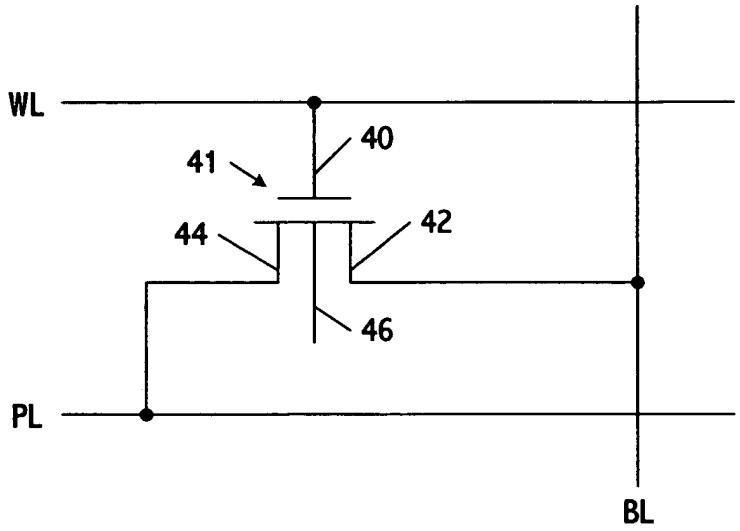

FIG. 6A

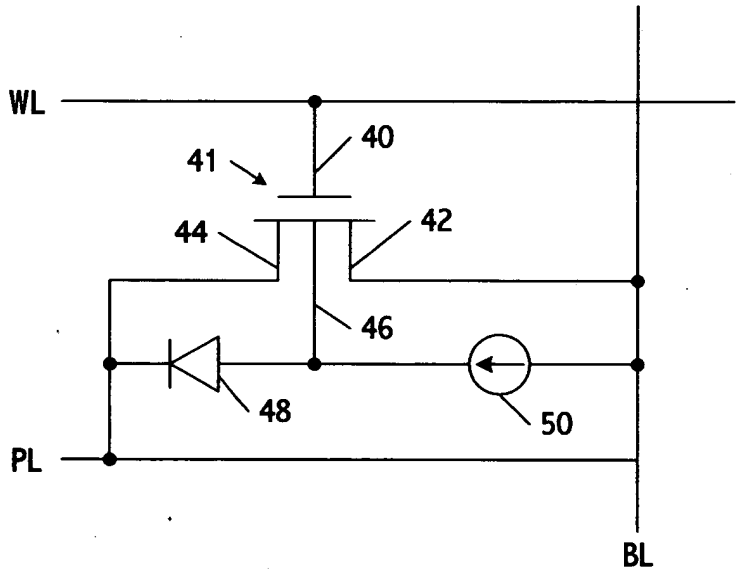

FIG. 6B

	SECOND CHANNEL INTERFACE (PURGE LINE)	GATE (WORD LINE)	FIRST CHANNEL INTERFACE (BIT LINE)
HOLD	LOW	LOW	LOW OR HIGH
PURGE	VERY LOW	VERY LOW	LOW
WRITE 0	LOW	HIGH	LOW
WRITE 1	LOW	HIGH	HIGH

FIG. 7